

# Process C1210

## CMOS 1.2 $\mu$ m

### Zero Threshold Devices

#### Electrical Characteristics

T=25°C Unless otherwise noted

<b>N-Channel Transistor</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>	<b>Comments</b>
Threshold Voltage	$V_{T_N}$	0.55	0.75	0.95	V	100x1.2 $\mu$ m
Body Factor	$\gamma_N$		0.34		$V^{1/2}$	100x1.2 $\mu$ m
Conduction Factor	$\beta_N$	64	75	86	$\mu A/V^2$	100x100 $\mu$ m
Effective Channel Length	$L_{eff_N}$	0.8	1.0	1.2	$\mu$ m	100x1.2 $\mu$ m
Width Encroachment	$\Delta W_N$		0.6		$\mu$ m	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

<b>Zero Vt N-Channel Transis.</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>	<b>Comments</b>
Threshold Voltage	$V_{T_{ZLN}}$	0.00	0.15	0.30	V	100x100 $\mu$ m
Body Factor	$\gamma_{ZLN}$		0.348		$V^{1/2}$	100x100 $\mu$ m
Conduction Factor	$\beta_{ZLN}$	75	90	105	$\mu A/V^2$	100x100 $\mu$ m
Saturation Current	$I_{DSATZN}$	28	34	40	mA	100x1.5 $\mu$ m

<b>P-Channel Transistor</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>	<b>Comments</b>
Threshold Voltage	$V_{T_P}$	-0.7	-0.9	-1.1	V	100x1.2 $\mu$ m
Body Factor	$\gamma_P$		0.38		$V^{1/2}$	100x1.2 $\mu$ m
Conduction Factor	$\beta_P$	21	25	29	$\mu A/V^2$	100x100 $\mu$ m
Effective Channel Length	$L_{eff_P}$	0.9	1.1	1.3	$\mu$ m	100x1.2 $\mu$ m
Width Encroachment	$\Delta W_P$		0.8		$\mu$ m	Per side
Punch Through Voltage	$BVDSS_P$	-9.0			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-10.0			V	

<b>Zero Vt P-Channel Transis.</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>	<b>Comments</b>
Threshold Voltage	$V_{T_{ZLP}}$	-0.3	-0.1	0.1	V	100x100 $\mu$ m
Body Factor	$\gamma_{ZLP}$		0.36		$V^{1/2}$	100x100 $\mu$ m
Conduction Factor	$\beta_{ZLP}$	21	26	31	$\mu A/V^2$	100x100 $\mu$ m
Saturation Current	$I_{DSATZP}$	-11	-15	-19	mA	100x1.5 $\mu$ m

# Process C1210

## Electrical Characteristics

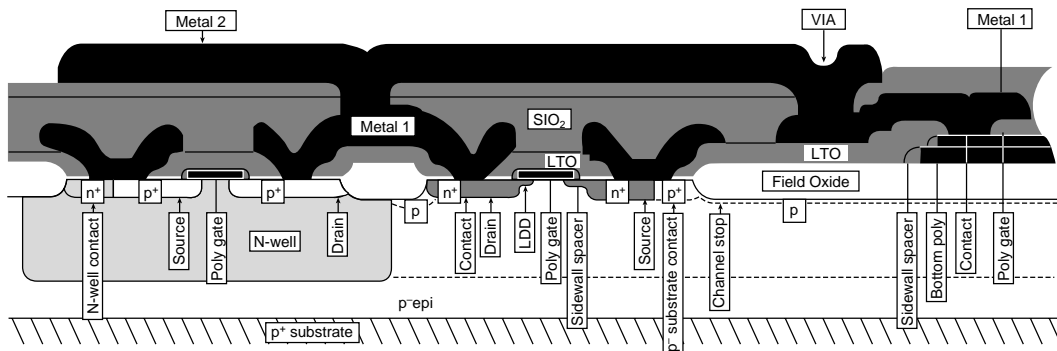
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well}(f)}$	0.6	1.0	1.3	K $\Omega/\square$	n-well
N+ Sheet Resistance	$\rho_{N+}$	20	35	50	$\Omega/\square$	
N+ Junction Depth	$x_{jN+}$		0.35		$\mu\text{m}$	
P+ Sheet Resistance	$\rho_{P+}$	50	75	100	$\Omega/\square$	
P+ Junction Depth	$x_{jP+}$		0.35		$\mu\text{m}$	
Gate Oxide Thickness	$T_{GOX}$		24		nm	
Field Oxide Thickness	$T_{FIELD}$		800		nm	
Gate Poly Sheet Resistance	$\rho_{POLY2}$	15	22	30	$\Omega/\square$	
Bottom Poly Sheet Res.	$\rho_{POLY1}$		35		$\Omega/\square$	
Metal-1 Sheet Resistance	$\rho_{M1}$		50		m $\Omega/\square$	
Metal-2 Sheet Resistance	$\rho_{M2}$		30		m $\Omega/\square$	
Passivation Thickness	$T_{PASS}$		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	$C_{OX}$	1.28	1.38	1.58	fF/ $\mu\text{m}^2$	
Metal-1 to Poly-1	$C_{M1P}$		0.057		fF/ $\mu\text{m}^2$	
Metal-1 to Silicon	$C_{M1S}$				fF/ $\mu\text{m}^2$	
Metal-2 to Metal-1	$C_{MM}$		0.035		fF/ $\mu\text{m}^2$	
Poly-1 to Poly-2	$C_{P1P2}$	0.69	0.86	1.03	fF/ $\mu\text{m}^2$	

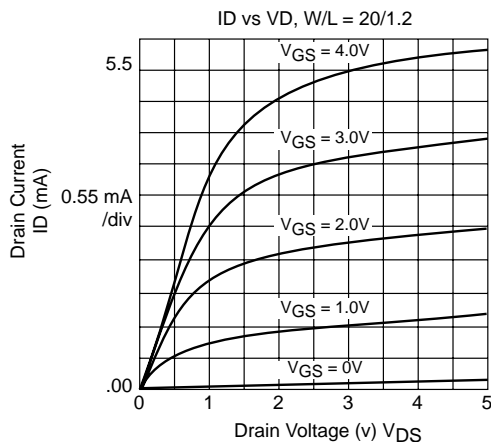
## Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.5/ 2.0 $\mu$ m
Starting Mat. Resistivity	7 - 8.5 $\Omega$ -cm	N+ To P+ Space	9.0 $\mu$ m
Typ. Operating Voltage	5V	Contact To Poly Space	1.5 $\mu$ m
Well Type	N-well	Contact Overlap Of Diffusion	1.0 $\mu$ m
Metal Layers	2	Contact Overlap Of Poly	1.0 $\mu$ m
Poly Layers	2	Metal-1 Overlap Of Contact	1.0 $\mu$ m
Contact Size	1.5x1.5 $\mu$ m	Metal-1 Overlap Of Via	1.0 $\mu$ m
Via Size	1.5x1.5 $\mu$ m	Metal-2 Overlap Of Via	1.0 $\mu$ m
Metal-1 Width/Space	2.5 / 1.5 $\mu$ m	Minimum Pad Opening	65x65 $\mu$ m
Metal-2 Width/Space	2.5 / 1.5 $\mu$ m	Minimum Pad-to-Pad Spacing	5.0 $\mu$ m
Gate Poly Width/Space	1.5 / 2.0 $\mu$ m	Minimum Pad Pitch	80.0 $\mu$ m

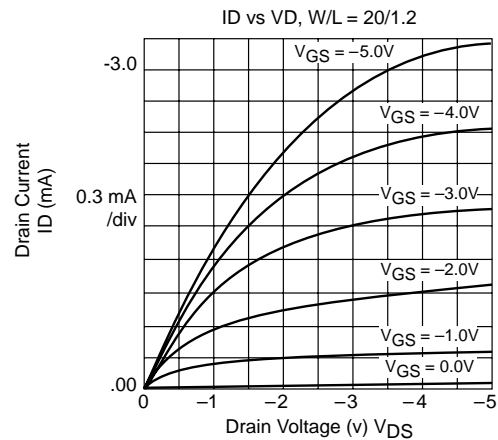
Special Feature of C1210 Process: This process offers zero threshold n- and p-channel transistors in addition to normal threshold transistors of CMOS 1.2 $\mu$ m technology.



Cross-Sectional view of the LVMOS process



n-ch Transistor IV characteristics of a 20/1.2 device



p-ch Transistor IV characteristics of a 20/1.2 device

